REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-8 are now in the application. Claim 1 has been amended. Claim 8 has been added. Claims 4-7 have been allowed.

In the section entitled "Claim Rejections - 35 USC § 102" on pages 2-5 of the above-mentioned Office action, claims 1-3 have been rejected as being anticipated by Horak et al. (US 6,063,658) under 35 U.S.C. § 102(b).

The rejection has been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found in Figs. 3-6 of the drawings and the corresponding description on pages 10-12 of the specification.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> applying a sacrificial layer made from a material selectively etchable with respect the storage layer and to polysilicon onto the storage layer;

producing openings in the sacrificial layer, the storage layer, and the lower boundary layer, extending to the semiconductor body, the openings being produced above regions where buried bit lines are to be produced;

...

applying an upper boundary layer on a surface of the storage layer and the residual portion of the polysilicon and oxidizing the residual portion of the polysilicon to form an oxide region, the oxide region being thicker than the lower boundary layer, the lower boundary layer, the storage layer and the upper boundary layer acting as a gate dielectric;

forming a diffusion region in the semiconductor body below the oxide region during the oxidation of the residual portion of the polysilicon, the diffusion region forming the buried bit line.

Horak et al. describe a method of making DRAM cells including a trench, which is filled with doped polysilicon. Fig. 1 of Horak et al. shows a standard DRAM cell according to the state of the art. According to the detailed description in column 2, lines 44-51 of Horak et al., Fig. 1 shows source and drain regions 9, 11, a deep trench capacitor 1 and a so-called buried strap 12 that connects the deep trench capacitor storage node 1 to the source/drain diffusion 11. Horak et al. modify this structure to provide a structure as shown in Fig. 2, in which the cross section of the gate oxide is shown to have an L-shape and the buried strap 19 is highly n-doped and seems to substitute for the drain region 11.

A comparison of Figs. 2, 6, and 7 of Horak et al. does not indicate that the n-polysilicon in the trench is provided as a source/drain region or even as a bitline. Instead, the bitlines are applied on top of the source diffusion 23, located on the opposite side of the gate with respect to the deep trench. The oxide-nitride-oxide layer sequence 112, 114, and 116 is not intended as a storage layer, and the arrangement of this layer sequence shows that it is not provided as the gate dielectric. Figs. 6 and 7 show that the trench filling is covered with the gate oxide 143. The formation of the gate oxide 143 is described in column 7, lines 24-27. A sacrificial oxide can be applied to remove any silicon surface damages before growing the gate oxide (see column 7, lines 17-24). No portion of the polysilicon filing is oxidized in the method of Horak et al. The passage in column 6, lines 23-24 cited by the Examiner on page 4 of the office action also does not describe an oxidation step.

The sacrificial layer of the method of the invention of the instant application is applied to limit the deposition of the polysilicon to the area in which the oxide region 6 is to be produced. This is completely different from the sacrificial oxide mentioned in column 7, lines 17-23 of Horak et al. in which the sacrificial oxide is used to remove any silicon surface damage before growing the gate oxide.

Clearly, Horak et al. do not show "applying a sacrificial layer made from a material selectively etchable with respect the storage layer and to polysilicon onto the storage layer; producing openings in the sacrificial layer, the storage layer, and the lower boundary layer, extending to the semiconductor body, the openings being produced above regions where buried bit lines are to be produced; ... applying an upper boundary layer on a surface of the storage layer and the residual portion of the polysilicon and oxidizing the residual portion of the polysilicon to form an oxide region, the oxide region being thicker than the lower boundary layer, the lower boundary layer, the storage layer and the upper boundary layer acting as a gate dielectric; forming a diffusion region in the semiconductor body below the oxide region during the oxidation of the residual portion of the polysilicon, the diffusion region forming the buried bit line," as recited in claim 1 of the instant application.

Claim 8 has been added to recite the optional step of producing spacers 12 at the walls of the openings 8 before the deposition of the polysilicon 11 in order to accurately set the trench width. The support for claim 8 may be found in Fig. 4 as well as page 10, line 23 to page 11, line 2 of the specification. Claim 8 is believed to be patentable because

none of the cites references discloses this feature as well as because claim is dependent on claim 1, which is believed to be patentable as discussed above.

Applicants acknowledge the Examiner's statement in the section entitled "Allowable Subject Matter" on page 5 of the above-mentioned Office action that claims 4-7 are allowed.

In view of the foregoing, reconsideration and allowance of claims 1-3 and 8 and an early issuance of a Notice of Allowance to claims 1-8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to

the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants

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